Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

G:\logo and QP Template\logo 3 Feb 2018 final.tif

**End Semester Examination – Nov/Dec – 2018**

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
| **Code :** | **14EC2067** | **Duration :** | **3hrs** |
| **Sub. Name :** | **VERILOG HDL** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Outline in detail about the Integer, Real and Time Register Data types in Verilog with suitable examples. | CO2 | 8 |
| b. | Illustrate about 8X1 mux and invent the behavioral modeling (using CASE Statement) using Verilog. | CO2 | 6 |
| c. | Discuss about the data types including Value Set,Nets,Registers and Data Types in Verilog. | CO2 | 6 |
| (OR) | | | | |
| 2. | a. | Demonstrate in detail about the design of full adder and write the gate-level modeling using Verilog. | CO2 | 8 |
| b. | Illustrate about two types of Design Methodologies. | CO1 | 6 |
| c. | Design full subtractor and invent the gate-level modeling using Verilog. | CO2 | 6 |
|  |  |  |  |  |
| 3. | a. | Illustrate a Verilog code for a counter which increments the count from 0 to 127 and exit at count 128 using while loop. | CO3 | 2 |
| b. | X=4’b0011; Y=4’b1011;Z=4’b x011;  Determine :  X & Y  X^~Y  X&Z  X^Y | CO1 | 2 |
| c. | Apply reduction operation:  A=4’b0101; B=4’b0110;  | B, &B, ~ ^ A, | A | CO1 | 2 |
| d. | Illustrate about the different types of Gate delays. | CO1 | 4 |
| e. | Design a 4-bit ripple counter using negative edge triggered flip-flops. | CO3 | 10 |
| (OR) | | | | |
| 4. | a. | Estimate about always and initial statement in behavioral modeling. | CO2 | 12 |
| b. | Design  using CMOS Logic and write switch level Verilog Description. | CO3 | 8 |
|  |  |  |  |  |
| 5. | a. | Elaborate in detail about MOS Switches, CMOS Switches and Resistive Switches. | CO3 | 10 |
| b. | Develop a Switch-Level Verilog Description of CMOS Flip-flop. | CO3 | 10 |
| (OR) | | | | |
| 6. | a. | Determine about always and initial statement in behavioral modeling. | CO2 | 12 |
|  | b. | Distinguish the different operators used in Verilog. | CO2 | 8 |
|  |  |  |  |  |
| 7. | a. | Develop a Switch-Level Verilog Description of 2-to-l Multiplexer. | CO3 | 8 |
| b. | Design switch level modeling of CMOS NAND Gate. | CO3 | 8 |
| c. | Summarize the function of Concatenation Operator. | CO2 | 4 |
| (OR) | | | | |
| 8. |  | Design Finite State Machine for Newspaper Vending Machine and write the Verilog Description. | CO3 | 20 |
|  | |  |  |  |
|  | | **Compulsory**: |  |  |
| 9. | a. | With neat examples describe about AND/OR and Buf/NOT Gates under Gate Modeling. | CO2 | 12 |
| b. | Discuss about test bench and develop the test bench for 4-to-1 Multiplexer. | CO3 | 8 |